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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PHAM, THANH V

ART UNIT PAPER NUMBER

2823

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/709,483

Applicant(s)

KWON, OH-NAM

Examiner

Thanh V. Pham

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment filed 11/13/2006 is sufficient to overcome the rejection of claims 1-12 based upon description and enablement requirement under 35 U.S.C. 112, first paragraph.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. US 5,247,191 in combination with Shigeta et al. US 6,480,253 B1, Havemann et al. U.S. Patent No. 5,891,804 and Zhao et al. US 5,660,706.

The Yamazaki et al. reference discloses an improved method for filling trench in a single layer substrate to produce electrode for LCD devices. Embodiment 3 comprises preparing a substrate; forming a photoresist pattern P1 on the substrate; etching a portion of the substrate to form a groove 101 beneath a top surface of the substrate using the photoresist pattern P1 as a mask; depositing a metal 102 on the substrate, a height of the second metal being smaller than a depth of the groove; removing the photoresist pattern on the substrate and the second metal on the photoresist other than in the groove *by lift-off technique (col. 6, line 4), fig. 7(A).*

The Yamazaki et al. reference does not teach how the lift-off technique is applied so that the height of the metal being smaller than a depth of the trench is obtained.

The Shigeta et al. reference teaches forming electrode for LCD device in trench 10, figs. 3 wherein the metal 3 is formed in trench 10 with a height of the metal being smaller than a depth of the trench, *a side portion of the photoresist pattern being exposed between the substrate and the metal*; and the photoresist pattern on the substrate and the second metal on the photoresist other than in the trench is removed *by lift-off process, col. 8, lines 19-42.*

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the lift-off technique of Yamazaki et al. with the lift-off process of Shigeta et al. because the process of Shigeta et al. would enable the process steps of Yamazaki et al. in order to have *a side portion of the photoresist pattern being exposed between the substrate and the metal.*

The Yamazaki et al./ Shigeta et al. combination does not disclose preparing a mixed solution having a reductant and a first metal for forming the first metal on the second metal in the groove by submerging the substrate in the mixed solution so that the formed metal line having "a surface including the surface of the substrate and the surface of the first metal is substantially planar".

The Havemann et al. reference discloses a process for forming thin film conductors comprising forming a photoresist pattern 46 on a substrate 42/40; etching a portion of the substrate to form a groove 47 *beneath a top surface of the glass substrate* using the photoresist pattern as a mask; depositing a second metal 50 on the substrate, col. 2, lines 13-15, and a height of the second metal being smaller than a depth of the groove, fig. 3b; removing the photoresist pattern on the substrate and the second metal

on the photoresist other than in the groove, fig. 3c; and forming the first metal 52 principally copper, col. 2, line 18, on the second metal in the groove, col. 4, lines 54-55, by electroless plating.

Further, the Zhao et al. reference discloses, col. 1, lines 46-60

One technique for depositing copper, as well as other metals, is electroless deposition. In comparison to other copper deposition techniques, electroless copper deposition is attractive due to the low processing cost and high quality of copper deposited. ...

In addition, electroless deposition of copper (as well as other metals), offers an advantage in the selective growth of the metal in an interconnect opening (such as a via opening). Selective growth eliminates the need for a polishing or etching step to remove the excess deposited material. Techniques for selective deposition are known in the art

The step of electroless deposition inherently includes the step of preparing a mixed solution having a reductant and a first metal and submerging the substrate in the mixed solution.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method steps of Havemann modified with the selective electroless deposition step in Zhao et al. into the method of Yamazaki et al./ Shigeta et al. combination as those formation steps would have been selected to eliminate the need for a polishing or etching step to remove the excess deposited material and to improve further the filling trench in accordance with the thin film conductor as taught by the Yamazaki et al./ Shigeta et al. combination. The selective deposition as taught by Zhao et al. would provide "a surface including the surface of the substrate and the surface of the first metal is substantially planar" (figs. 12-13).

4. Claims 3, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al./ Shigeta et al. and Havemann et al./Zhao et al. combination as applied to claims 1-2 and 11 above, and further in view of Charneski et al. U.S. Patent No. 6,284,652 B1 and/or Eriksson U.S. Patent No. 3,632,435.

The above combination discloses substantially all of the instant invention.

However, both Yamazaki et al./ Shigeta et al. and Havemann et al./Zhao et al. do not disclose the mixed solution for the electroless plating.

The Charneski et al. reference discloses sulfuric acid and cupric sulfate (col. 8, line 31) used in cooper plating process.

The Eriksson reference discloses the use of silver nitrate, gold chloride with noble metal salts and hydroxide in the mixed solution for electroless plating (col. 5, lines 45-65).

It would have been obvious to one of ordinary skill in the art to apply the known materials as stated by Charneski et al. and/or Eriksson to the method of Yamazaki et al./ Shigeta et al. and Havemann et al./Zhao et al. combination because such materials would have been chosen for the electroless plating process in the art of making electrode for an electronic device in the process of Yamazaki et al./ Shigeta et al. and Havemann et al./Zhao et al. combination. The use of sulfuric acid and cupric sulfate is well known to those skills in the art as taught by Charneski et al. and/or Eriksson.

5. Claims 4-5, 7-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the above combination as applied to claims 1-3, 6, 9 and 11 above, and further in view of Senda et al. U.S. Patent No. 5,364,459.

Re claims 1-3, 6, 9 and 11, the combination discloses essentially all of the invention, it does not disclose Ag and Au for the metal and the kind of reductant used.

Re claims 2, 4-5, 7-8, 10-11, the Senda et al. reference discloses in the background of the invention that the first metal could be Cu, Ag or Au; the reductant could be formaldehyde; and "the electroless plating is not only applied to formation of a conductive film such as an electrode for an electronic component", col. 1, lines 10-35.

It would have been obvious to one of ordinary skill in the art to apply the known materials as stated by Senda et al. to the method of the combination because such materials would have been chosen for electroless plating process in order to have better trench fill in the art of making electrode for an electronic device. The use of Cu, Ag or Au and formaldehyde is well known to those skilled in the art as taught by Senda et al.

6. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann et al./ Yamazaki et al./ Shigeta et al./Senda et al. and Charneski et al. and/or Eriksson combination as applied to claims 1-11 above, and further in view of JP 05-265040 (provided by applicant) and applicant's admitted prior art.

In the combination, the Havemann et al. reference discloses a process for forming thin film conductors comprising forming a photoresist pattern on a substrate

using electroless plating, the Senda et al. reference discloses formation of a conductive film such as an electrode for an electronic component using electroless plating.

None of the references disclose the further steps for forming the transistor.

However, JP 05-265040 discloses the steps of making gate line in a trench and the applicant admitted prior art performs the further steps for forming the transistor.

It would have been obvious to one of ordinary skill in the art to provide the method of the combination the further step of making a trench gate line of the JP 05-265040 and the further step of forming a transistor of applicant's admitted prior art as the method and the analogous electrode would be selected in accordance with the teaching of JP 05-265040 and the applicant's admitted prior art to complete the LCD device.

Response to Arguments

7. Applicant's arguments filed 01/13/2006 have been fully considered but they are not persuasive.

8. Applicant argues that none of the cited references and applicant's admitted prior art disclose or suggest "the first metal on the second metal is at substantially the same height as the substrate, and wherein a surface including the surface of the substrate and the surface of the first metal is substantially planar" then points to Zhao with the argument that "Figs. 12 and 13 of Zhao illustrate only a cross section portion of the structure - the top, bottom, left and right ends of the [in] Figs. 12 and 13 are not the actual ends of the structure. Accordingly, Zhao does not disclose or suggest 'a surface

including the surface of the dielectric 56 and the copper 52c is planar,' as alleged by the Examiner". The examiner does not agree with that conclusory statement simply because Zhao's figs. 12 and 13 clearly show 'a surface including the surface of the dielectric 56 and the copper 52c is planar'. In Zhao's figs., the curvilinear lines are the same as applicant's curvilinear lines in instant figs. 5A – 6B. Both do not need to show the actual ends of the structure and still be understandable.

9. In response to applicant's argument that "the references teach in different directions, there would not have been any motivation to combine them", the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Further, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, the first combination in the rejection is up to the first five steps of the instant claimed invention in claim 1 wherein the lift-off technique is applied so that the height of the metal being smaller than a depth of the trench is obtained. The Yamazaki

et al. reference teaches removing the photoresist pattern on the substrate and the second metal on the photoresist other than in the groove *by lift-off technique* but does not shows how the lift-off technique is applied and the Shigeta et al. reference shows the photoresist pattern on the substrate and the second metal on the photoresist other than in the trench is removed *by lift-off process*, detailing at least in figs. 3. Both produce electrode for LCD devices.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



01/24/2006


George Foursor
Primary Examiner